CDB4272

Evaluation Board For CS4272

Features

- Differential Analog Inputs
- CS8406 S/PDIF digital audio transmitter
- CS8416 S/PDIF digital audio receiver
- Header for optional external configuration of CS4272
- Header for external DSP serial audio I/O
- 3.3V to 5.0V Logic Interface
- Demonstrates recommended layout and grounding arrangements
- Microsoft Windows® compatible software interface to configure CS4272 and inter-board connections

ORDERING INFORMATION

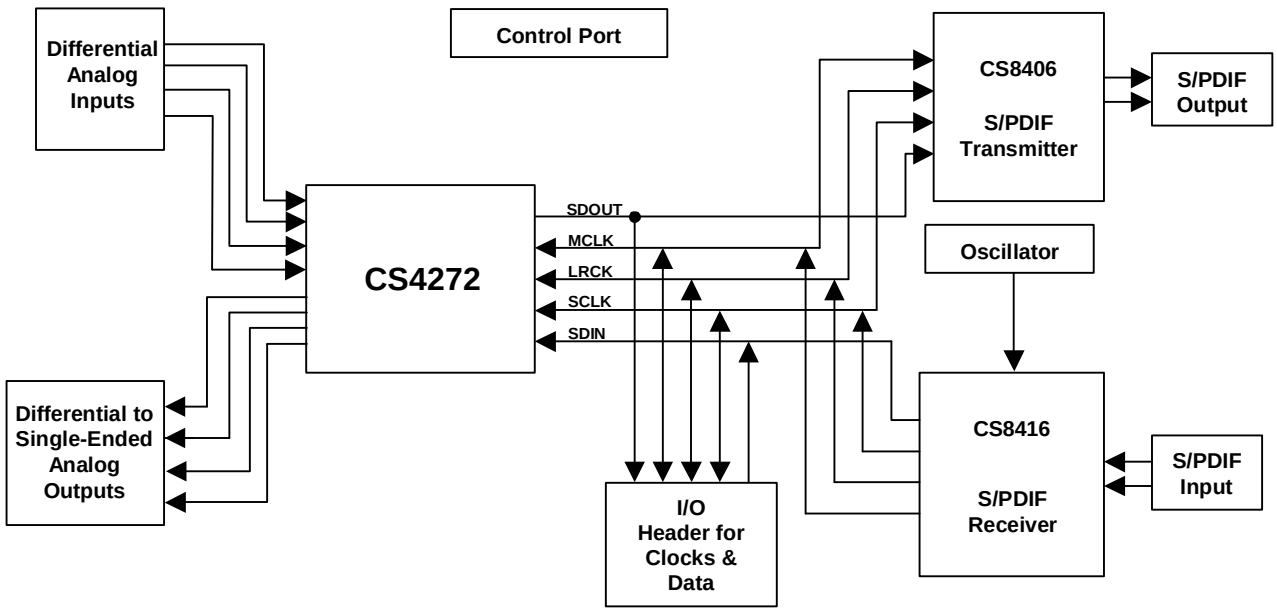
CDB4272 Evaluation Board

Description

The CDB4272 demonstration board is an excellent means for evaluating the CS4272 stereo CODEC. Evaluation requires an analog/digital signal source and analyzer, and power supplies. Optionally, a Windows® PC compatible computer may be used to evaluate the CS4272 in control port mode.

System timing can be provided by the CS4272, by the CS8416 phase-locked to its S/PDIF input, by an I/O stake header or by an on-board oscillator. RCA phono jacks are provided for the CS4272 analog outputs . Balanced XLR jacks are provided for the CS4272 analog inputs. Digital data I/O is available via RCA phono or optical connectors to the CS8416 and CS8406.

Microsoft Windows® software provides a GUI to make configuration of the board easy. The software communicates through the PC's parallel port to configure the hardware so that all features of the CS4272 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.



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1. SYSTEM OVERVIEW

The CDB4272 demonstration board is an excellent means for evaluating the CS4272 stereo CODEC. Analog and digital audio signal interfaces are provided, as well as a DB-25 computer parallel port interface for use with the supplied Window® configuration software.

The CDB4272 schematic set has been partitioned into 10 pages and is shown in Figures 6 through 15.

1.1 CS4272 Stereo Audio CODEC

A complete description of the CS4272 is included in the CS4272 product data sheet.

1.2 CS8406 Digital Audio Transmitter

The operation of the CS8406 transmitter (see Figure 11) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS4272 to the standard S/PDIF data stream. The CDB4272 is able to operate the CS8406 in either master or slave mode. The serial audio input data for the CS8406 is received from the serial audio output of the CS4272. Using the GUI, the user may elect to supply the CS8406 with an external serial audio data source through a stake header (J17). Digital Interface format selection of either Left Justified or I^2S can be made via the control port GUI or via the I2S/$\overline{LJ}$ position on switch, S1 (see Table 2 for switch control options).

1.3 CS8416 Digital Audio Receiver

The operation of the CS8416 receiver (see Figure 10) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS4272. The CDB4272 is able to operate the CS8416 in master or slave mode. Digital Interface format selection of either Left Justified or I^2S can be made via the I2S/$\overline{LJ}$ position on S1. Left Justified, I^2S or Right Justified interface formats can be selected via the control port GUI.

The CS8416 always sources an MCLK signal. As a result, it should be noted that the CS8416 will provide invalid data in modes where the MCLK signal is generated by the CS4272 or received through the stake header (J26). Care should be taken to ensure that the crystal (Y2) is removed when the board is configured to receive MCLK from the CS8416.

The CS8416 contains an internal input multiplexer which must be set to receive the appropriate stream from the Optical or Coaxial input connector. This may be done via the Coaxial/Optical position on S1, or through the control port GUI.

1.4 Canned Oscillator

Oscillator Y1 provides a System Clock (OMCK) to the CS8416. This clock can be routed through the CS8416 and out the RMCK pin by simply disconnecting the S/PDIF input. To use the canned oscillator as the source of the MCLK signal, configure the board to receive MCLK from the CS8416 using either the MCLK[1:0] positions on S1 or the GUI, and remove the input S/PDIF stream. Care should be taken to ensure that the crystal (Y2) is removed when the board is configured to receive MCLK from the canned oscillator.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.000 MHz crystal oscillator stuffed at Y1. Please refer to the CS8416 data sheet for details on OMCK operation.

1.5 Analog Input

XLR connectors supply the CS4272 analog inputs through unity gain, AC-coupled differential circuits. A 2 Vrms differential signal will drive the CS4272 inputs to full scale.

The CDB4272 was designed for use with not only the CS4272, but also the CS421 with a simple change of assembly options. For this reason, the input buffer schematic shown in Figure 8 reflects only the configuration assembled on the CDB4272. For a complete schematic of the analog input buffer printed on the PCB, refer to Figure 19

1.6 Analog Outputs

The CS4272 analog output is routed through a differential to single-ended, unity-gain low pass filter, which is AC-coupled to an RCA phono jack (see Figure 9). The analog output filter on the CDB4272 has been designed to add flexibility when evaluating the CS4272 DAC outputs. The output filter was designed in a two stage format, with the first stage being an optional instrumentation amplifier, and the second stage a 2-pole butterworth low pass filter.

The 2-pole low pass filter provides an example of an inexpensive circuit with good distortion and dynamic range performance. It is designed to have the in-band impedance matched between the positive and negative legs. It also provides a balanced to single-ended conversion for standard un-balanced outputs. Evaluate this circuit by placing the FILT jumpers (three per output channel) to position 1 (selectable by J13, J14 & J15 for AOUTR, etc.).

The instrumentation amplifier is optionally inserted before the LPF by changing the FILT jumpers to position 2. The instrumentation amplifier incorporates a 5x gain (+14 dB) which effectively lowers the noise contribution of the following 2-pole LPF. This improves the overall dynamic range of the system. The gain of this stage is determined from the following equation:

$$\text{Gain} = 1 + \frac{2(R)}{R_2}$$

The resistor designated by R2 (see Figure 1) can be adjusted to change the gain of the instrumentation amp. The feedback resistors 'R' on the two sides of the instrumentation amp must be equal.

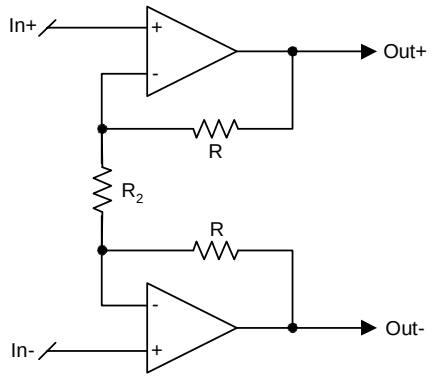


Figure 1. Instrumentation Amplifier Configuration

A resistor divider pad (parallel combination of R5 // R8 // R10 and R22 for AOUTR) has been placed after the low pass filter to bring the circuit back to unity gain (selectable with jumper J15 for AOUTR).

In the resistor divider pad, three 3.92 kΩ, 1/4 W, 1210 size resistors are used in parallel to provide a combined resistance of 1.30 kΩ and a combined power handling of 3/4 W. This is done to provide sufficient power handling capability to accommodate the high signal levels output from the instrumentation amplifier stage. When not using the instrumentation amplifier, these resistors may be reduced to a single 1.30 kΩ, 1/10 W, 0805 size resistor (for muting attenuation purposes).

In certain places throughout the output circuit, 1/8 W, 1206 size and 1/4 W, 1210 size resistors are used. Similar to the parallel resistors in the resistor divider pad, these are used to provide sufficient power handling capability in order to accommodate the high signal levels output from the instrumentation amplifier stage. When not using the instrumentation amplifier, these resistors may all be replaced with 1/10 W, 0805 size resistors.

The attenuation provided by the output mute transistor (Q2 for AOUTR) is determined by the resistor-divider formed between the collector-emitter on-resistance and the output resistance of the LPF (R5 // R8 // R10 for AOUTR). The greater the output resistance, the greater the attenuation will be for a given transistor. The trade off is that a high output impedance is not usually desirable, and may affect the voltage transfer to the next stage based upon its input impedance.

The same resistance that affects the transistor mute level also affects the HPF formed with the output DC-block capacitor (C26 for AOUTR). For LPF configuration 2, the values for the DC-block capacitor and output resistor pad (R5 // R8 // R10 and R22 for AOUTR) were chosen to minimize the rise in distortion performance at low frequency due to the electrolytic's

dielectric absorption properties. The HPF formed by this R-C pair must be such that the voltage across the aluminum electrolytic DC-block capacitor is minimal at 20 Hz. This keeps the distortion due to the electrolytic's dielectric absorption properties to a minimum. For a design utilizing only LPF configuration 1, there is no post-LPF resistor-divider pad, and a much smaller value capacitor can be used (22 µF).

Similar to the output DC-block capacitor described above, the value of the AC coupling capacitor from the non-inverting input of the 2-pole low pass to ground (C23 for AOUTR) was also chosen to minimize the rise in distortion performance at low frequency due to the electrolytic's dielectric absorption properties. These properties become apparent only as the signal level on that leg increases to the levels output from the differential amp used in LPF configuration 2. For a design utilizing only LPF configuration 1, the levels on that leg are sufficiently low, and a much smaller value capacitor can be used (22 µF).

1.7 Stand-Alone Control

Switch S1 allows stand-alone hardware signal routing and configuration of the CDB4272. See Table 2 for a list of the various options available. After changing settings using S1, the user must assert a reset by pressing the RESET button (S2).

Operation in stand-alone mode requires the parallel port cable to remain disconnected from the DB-25 connector (J31). Connecting a cable to the connector will enable the PC control port, automatically disabling switch S1 and its associated logic.

1.8 PC Parallel Port Control

A graphical user interface is included with the CDB4272 to allow easy manipulation of all registers of the CS4272 and hardware configuration of the CDB4272. Connecting a cable to the DB-25 connector (J31) will enable the PC control port, automatically disabling switch S1 and its associated logic.

1.9 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J26, J32, J17, and J24.

The 10-pin header, J26, allows the user bidirectional access to MCLK, SCLK, and LRCK. The direction of these signals is set using S1 (see Table 2 for switch control options) or the control port GUI. Also accessible from this header is a buffered version of the SDOUT signal from the CS4272, and a buffered input which, using S1 or the GUI, can be configured to drive the CS4272 SDIN pin. Care should be taken to ensure that the crystal (Y2) is removed when the board is configured to receive MCLK from this header.

The 2-pin header, J17, allows the user to supply the CS8406 with an external data source. This option is available through the control port GUI and may be asserted by setting the CS8406 data source to “Header”.

The 2-pin header, J24, supplies the user with a buffered version of the SDOUT signal generated by the CS8416. This may be used, for instance, to route received S/PDIF data off-board for processing before introducing it at the SDIN position on J26.

The 6-pin header, J32, allows the user bidirectional access to the SPI/I^2C control signals. The signals on J32 default to outputs. When a jumper is placed across J34, the header (J32) may be used as an input. When set as an input, the control signals on J32 are routed to the corresponding control pins on the CS4272 and external control signals may be applied.

1.10 Power

Power must be supplied to the evaluation board through at least three binding posts, +5.0 V (J1), +18.0 V (J6), and -18.0 V (J7). Jumper J10 allows the user to connect the VA supply of the CS4272 to a fixed +5.0 V supply or to another separate binding post (J5). Jumpers J8 and J9 connect the VL and VD supply, respectively, to a fixed +5.0 V or +3.3 V supply or to two separate binding posts (J2 and J3) for variable voltage settings. All voltage inputs must be referenced to the single black banana-type ground connector (see Figure 15).

It should be noted that devices other than the CS4272 are powered from the VL supply and therefore VL must be limited to a minimum of 3.3 V.

WARNING:Please refer to the CS4272 data sheet for allowable voltage levels.

1.11 Grounding and Power Supply Decoupling

The CS4272 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 5 provides an overview of the connections to the CS4272,
Figure 16 shows the component placement, Figure 17 shows the top layout, and Figure 18 shows the bottom layout. The decoupling capacitors are located as close to the CS4272 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V - J1	Input	+5.0 V Power Supply
-18V - J7	Input	-18.0 V to -5.0 V Power Supply for the op-amps
+18V - J6	Input	+5.0 V to +18.0 V Power Supply for the op-amps
VA - J5	Input	+5.0 V Power Supply for VA
VD - J3	Input	+3.3 V to +5.0 V Variable Power Supply for VD
VL - J2	Input	+3.3 V to +5.0 V Variable Power Supply for VL
GND - J4	Input	Ground Reference
RX-COAX - J25	Input	Digital audio input via coaxial cable
RX-OPT - OPT1	Input	Digital audio input via optical cable
TX-COAX - J12	Output	CS8406 digital audio output via coaxial cable
TX-OPT - J18	Output	CS8406 digital audio output via optical cable
PC Port - J31	Input/Output	Parallel connection to PC for SPI / I^2C control port signals and system configuration
PCM HEADER - J26	Input/Output	I/O for Clocks & Data
8416 SDOUT - J24	Output	CS8416 serial data output (SDOUT)
8406 SDIN - J17	Input	External data source for CS8406 SDIN
EXT CTRL I/O	Input/Output	I/O for external SPI / I^2C control port signals (J32) and control signal header in/out selection (J34)
AINL - J33 AINR - J30	Input	XLR jacks for differential analog input signal to CS4272
AOUTL - J23 AOUTR - J16	Output	RCA phono jacks for analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
M/S[1:0] (S1)	Subclock Master/Slave Select	*00 01 10 11	CS4272 is Master CS8416 is Master CS8406 is Master PCM Header, J26, is Master
MCLK[1:0] (S1)	Master Clock Source Select	*00 01 10 11	CS8416 Provides MCLK CS4272 Provides MCLK PCM Header, J26, Provides MCLK PCM Header, J26, Provides MCLK
Header/$\overline{8416}$ (S1)	CS4272 SDIN Source Select	*0 1	CS8416 Provides SDIIN PCM Header, J26, Provides SDIN
$\overline{Coaxial}$/ Optical (S1)	Optical or Coaxial S/PDIF Input Select	*0 1	Optical Input Coaxial Input
I2S/$\overline{LJ}$ (S1)	Digital Interface Format Select	*0 1	Left Justified, 24-bit I^2S, 24-Bit
128/$\overline{256}$ (S1)	Master Clock Speed Select	*0 1	256*Fs 128*Fs
M[1:0] (S1)	CS4272 Speed Mode Select	00 *01 10 11	Single-Speed Mode, with De-emphasis Single-Speed Mode, w/out De-emphasis Double-Speed Mode Quad-Speed Mode
J11, J19	Selects LED or Mute Circuit for AOUTA, AOUTB	1 *2	Mute Circuit Affects Analog Output Mute Circuit Disconnected (LED displays x$\overline{MUTEC}$ status)
J10	Selects source of voltage for the VA supply	*+5V ADJ	Voltage source is J1, +5.0 V binding post Voltage source is J5, VA binding post
J9	Selects source of voltage for the VD supply	*+5V +3.3V ADJ	Voltage source is J1, +5V binding post Voltage source is +3.3 V regulator Voltage source is J3, VD binding post
J8	Selects source of voltage for the VL supplies	*+5V +3.3V ADJ	Voltage source is J1, +5V binding post Voltage source is +3.3 V regulator Voltage source is J2, VL binding post
J13, J14, J15, J20, J21, J22	Selects DAC Output Filter	*1 2	Selects standard 2-pole filter Inserts instrumentation-amp and resistor divider.

*Default factory settings

Table 2. Jumper/Switch Settings

2. INITIAL BOARD SETUP

2.1 Power Supplies:

1) Verify that all power supplies are off before making connections.
2) Connect a +5.0 VDC power supply to the +5V (J1) red binding post. If correct configuration is other than the factory default, select VL and VD operating voltage by placing a jumper on J8 and J9 to select either +5.0 V or +3.3 V.
3) Connect a +18.0 to +5.0 VDC power supply to the +18V (J6) green binding post. If using the FILT position number 2 for the output filter stage, +18.0 V is required on J6.
4) Connect a -18.0 to -5.0 VDC power supply to the -18V (J7) yellow binding post. If using the FILT position number 2 for the output filter stage, -18.0 V is required on J7.
5) Connect the common ground of the power supplies to the GND (J4) binding post.
6) Attach all required analog and digital cables to the board jacks and connectors.
7) If software control is desired, attach parallel port cable between board and PC.
8) If using the External Control Header connection, attach the required user supplied flat ribbon cable to the header with the power supplies turned off.
9) With all cables and connections in place, turn on the power supplies to the board. Turn on supplies in this order: +5 V, +18 V, -18 V.
10) Press and release the RESET switch S2. The LED, D5, will illuminate as long as S2 is depressed indicating a reset condition. Once S2 is released, the LED should turn off. If it remains on, an error has occurred. At this point, power off the power supplies and recheck all connections. Apply power to the board and press and release S2. Once the LED has turned off, the board will be setup for use.

2.2 Installing the Software:

1) Create a directory called CDB4272 anywhere on your PC.
2) Copy CDB427X.exe from the included CD into this directory.
3) Run port95nt.exe from the CD. After running the program the system will need to be restarted.
4) If desired, create a shortcut to CDB427X.exe on your desktop. You should now be able to run CDB427X.exe. Double-click on CDB427X.exe or its shortcut.
5) Select the LPT port you are using to connect to the CDB4272.
6) Shut down the application, reset the board, and then restart the application.

2.2.1Verifying Board Operation:

1) If connected, disconnect the PC parallel cable.
2) Set all positions on S1 to LO, with the exception of M0 which should be set to HI.
3) Assert a reset by pressing the RESET button (S2).
4) Apply a S/PDIF input signal to the optical connector (OPT1). The converted signal should appear at the analog output jacks AOUTR and AOUTL.
5) Apply an analog input signal to the analog input jacks AINR and AINL. The converted signal should appear at the S/PDIF TX output jacks (J12 and J18).

3. CDB427X.EXE USER'S GUIDE

3.1 Main Window

The main window of the CDB4272 Graphical User Interface allows the user to view and change the configuration of the CS4272 and on-board configuration logic.

The Board Setup box contains all the controls necessary to manage clock and data routing and formats. To apply changes to the board, the “Send Board Setup” button must be pressed after making changes within the Board Setup box.

The CS4271/2 Setup box allows configuration of the internal registers of the CS4272. Changes made within this box will be reflected immediately. When in I^2C mode, the “Update” button will read the registers of the CS4272 and update the CS4271/2 Setup box to match.

3.2 Advanced Window

Clicking the “Advanced...” button on the main window will launch a graphical register map of the CS4272. Changes made to the register map will be immediately reflected in the main window, so you may wish to arrange them so that they do not obscure each other. When in I^2C mode, the “Update” button will read the registers of the CS4272 and update the Advanced Register Settings box to match. See Figure 3 below.

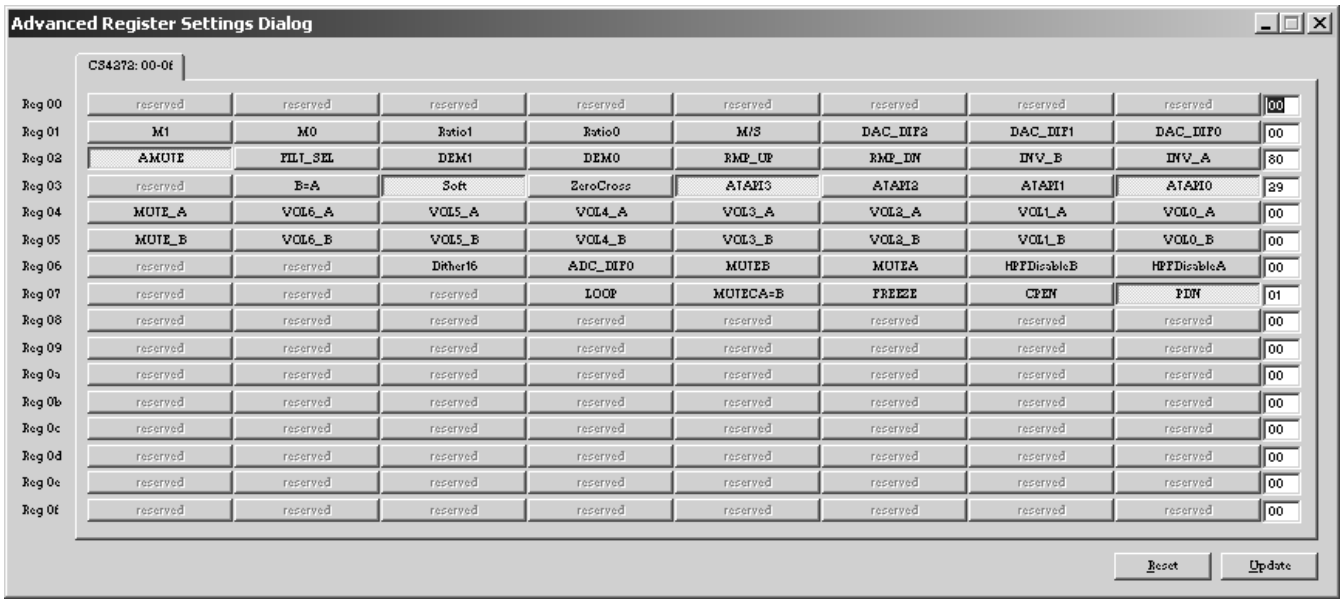

Advanced Register Settings Dialog
CS4272: 00-0f
Reg 00 reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 01 M1 M0 Ratio1 Ratio0 M/S DAC_DIF2 DAC_DIF1 DAC_DIF0 00
Reg 02 AMUTE FLT_SEL DEM1 DEM0 RMP_UP RMP_DN INV_B INV_A 80
Reg 03 reserved B=A Soft ZeroCross ATAPI3 ATAPI2 ATAPI1 ATAPI0 29
Reg 04 MUTE_A VOL6_A VOL5_A VOL4_A VOL3_A VOL2_A VOL1_A VOL0_A 00
Reg 05 MUTE_B VOL6_B VOL5_B VOL4_B VOL3_B VOL2_B VOL1_B VOL0_B 00
Reg 06 reserved reserved Dither16 ADC_DIF0 MUTEB MUTEA HPFDisableB HPFDisableA 00
Reg 07 reserved reserved reserved LOOP MUTECA=B FREEZE CPEN PDN 01
Reg 08 reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 09 reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0a reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0b reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0c reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0d reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0e reserved reserved reserved reserved reserved reserved reserved reserved 00
Reg 0f reserved reserved reserved reserved reserved reserved reserved reserved 00
Reset
Update

Figure 3. Advanced Window

3.3 I²C Mode No Acknowledge Error

The control port of the CS4272 requires the presence of an MCLK signal for correct operation. Because of this, if the board is set up to receive MCLK from a source that isn’t actively providing the signal, a no acknowledge error may result. This means that the GUI is expecting an acknowledgement from the CS4272, but isn’t receiving it. If this occurs, ensure that the appropriate source of MCLK is providing the signal. For example, if the board is set up to receive MCLK from the header, be sure that there is an active MCLK signal applied to the MCLK position on the header (J26). See Figure 4 below.

Figure 4. I²C Error Message

4. BLOCK DIAGRAM

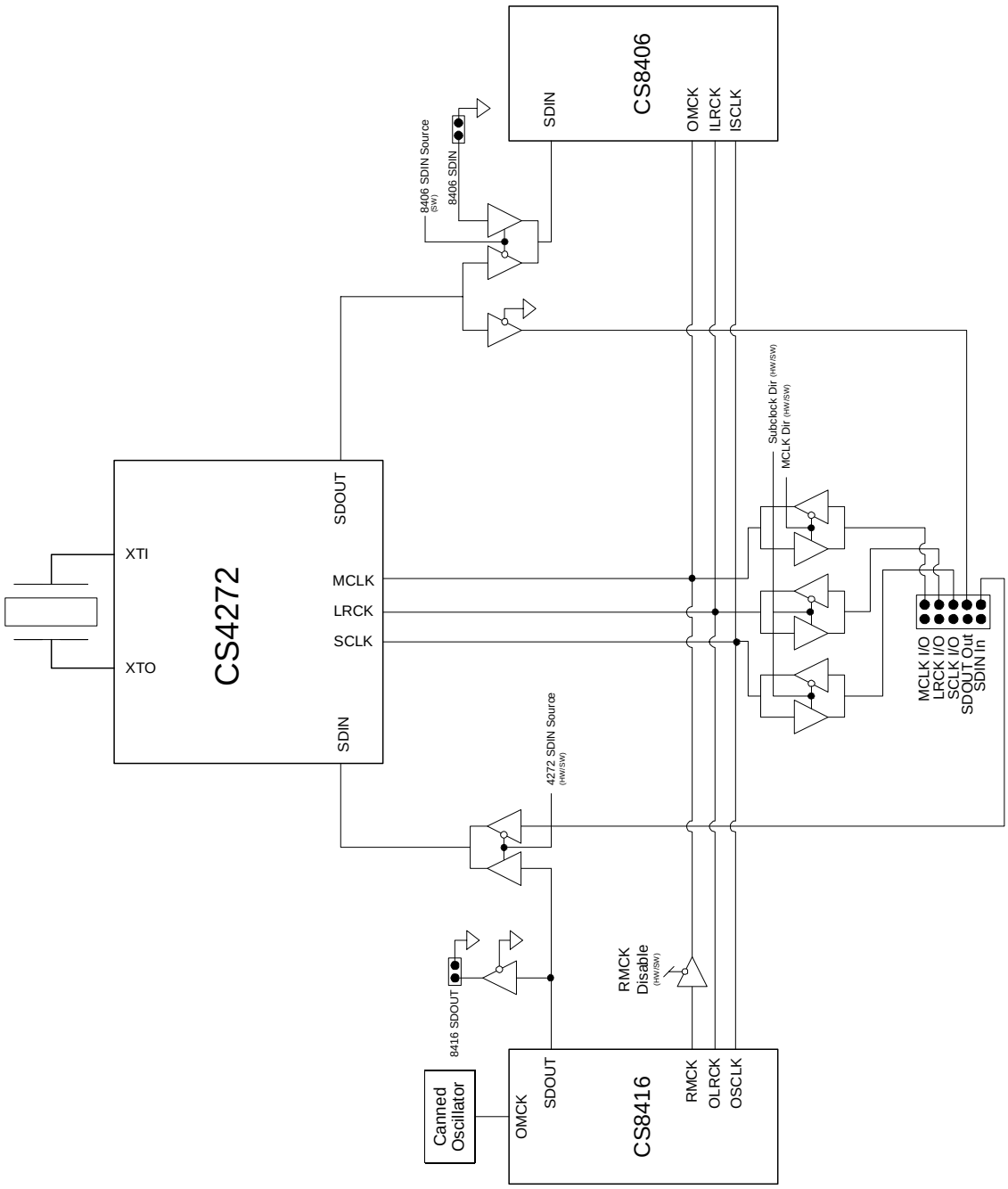


Figure 5. Clock and Data Routing

5. SCHEMATICS AND LAYOUT

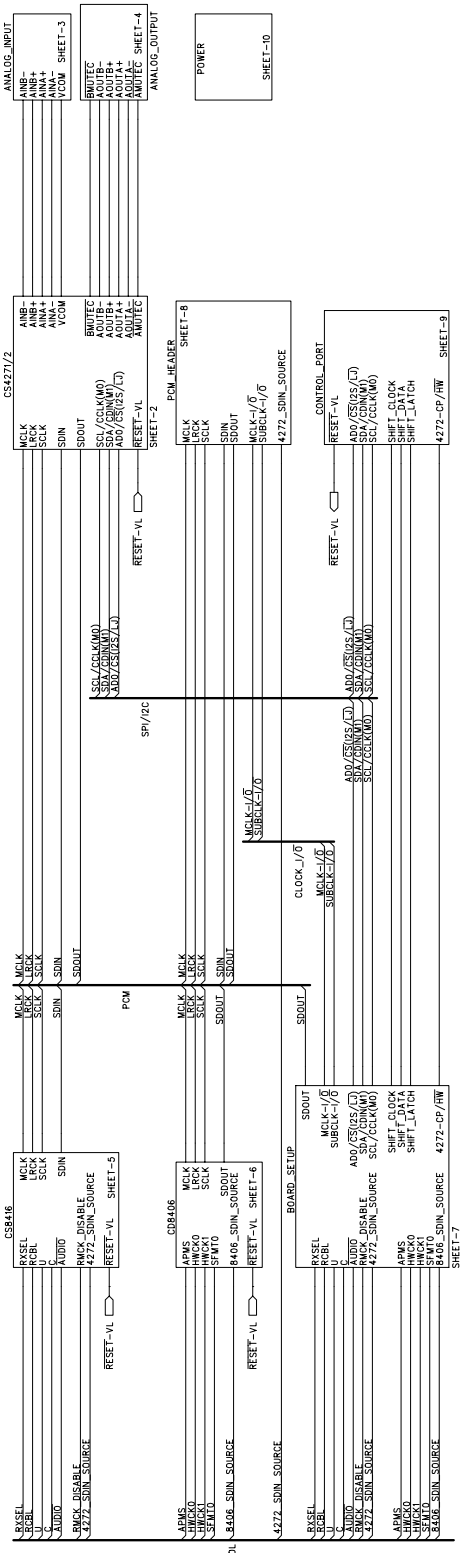


Figure 6. Hierarchy, Schematic Sheet 1

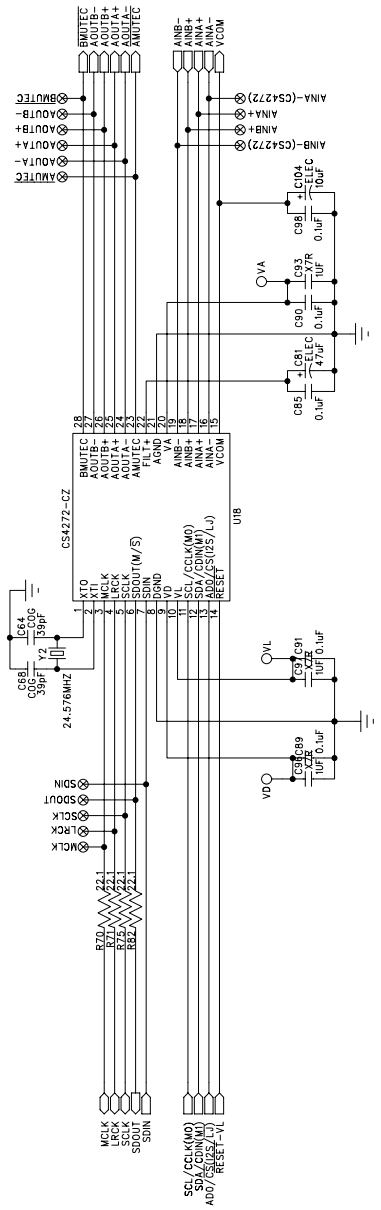
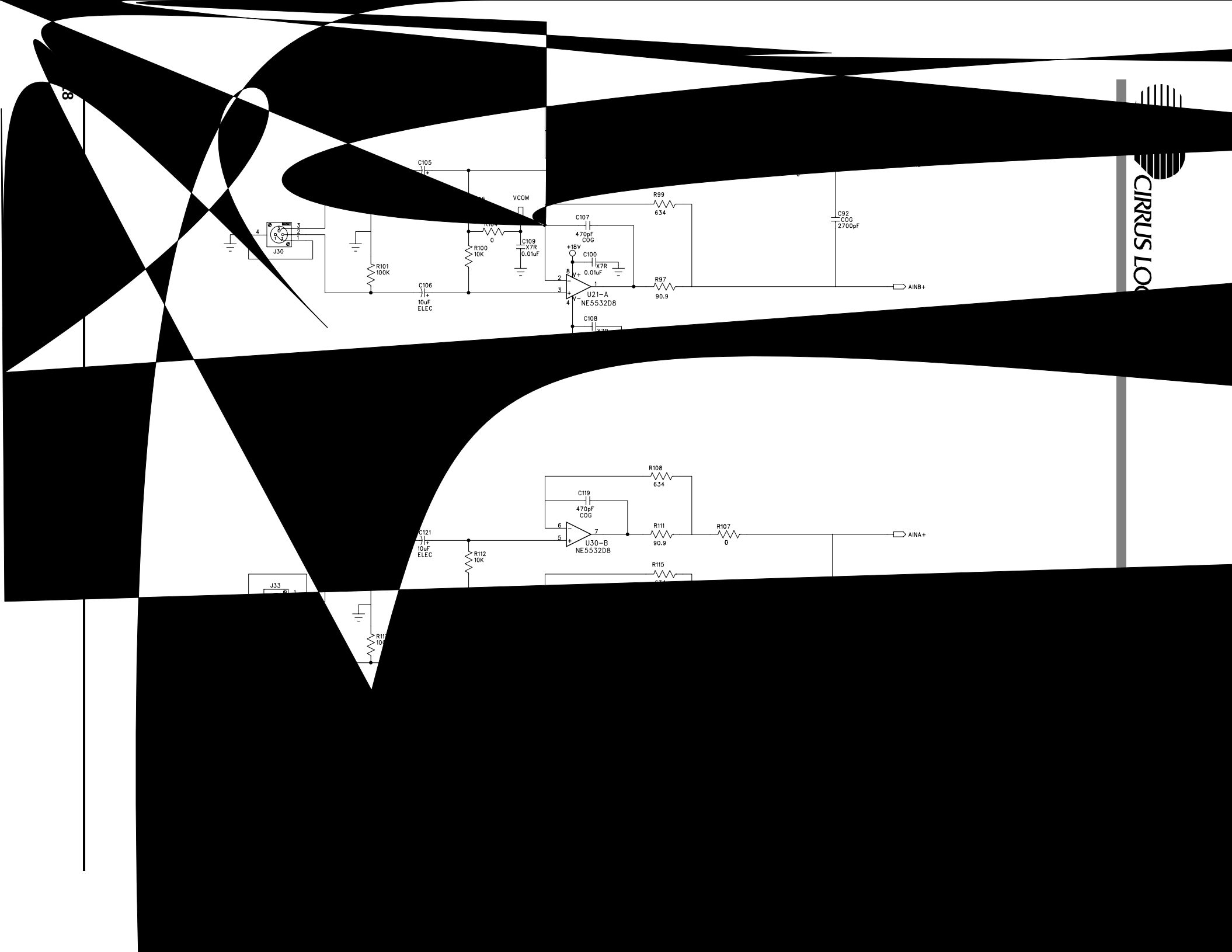


Figure 7. CS4272, Schematic Sheet 2


C105
VCOM
R99
634
C107
470pF
COG
C92
COG
2700pF
J30
R104
0
C109
X7R
0.01uF
+18V
C100
X7R
0.01uF
R100
10K
R101
100K
C106
10uF
ELEC
U21-A
NE5532D8
R97
90.9
AINB+
C108
R108
634
C119
470pF
COG
C121
10uF
ELEC
R112
10K
U30-B
NE5532D8
R111
90.9
R107
0
AINA+
R115
J33

8416 SDOUT

Selects Hardware Mode

Emphasis Off

Tx Passthrough Unused

Receiver Error

Select NVERR

96kHz - 192kHz PLL Filter Components From CS8416 Datasheet DS578PP2

In Stand-Alone Mode Use Coaxial/Opt

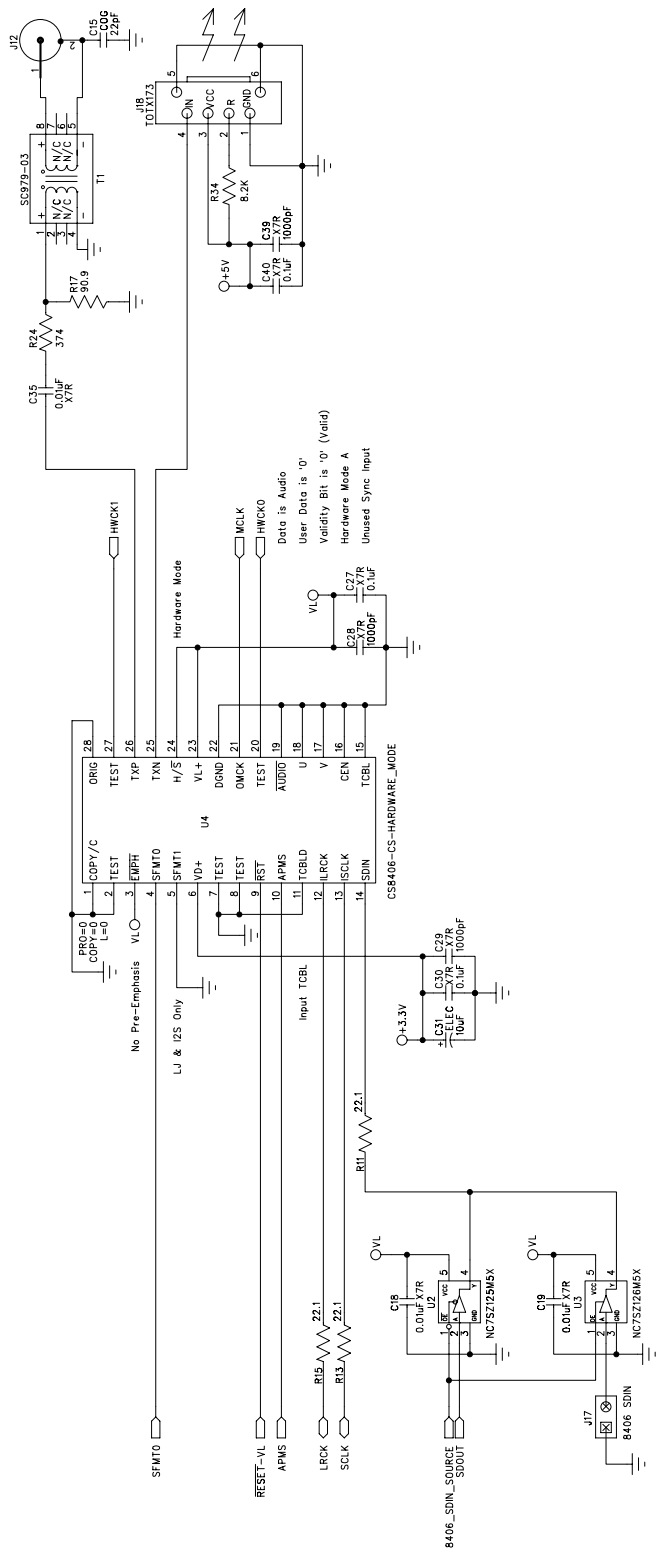
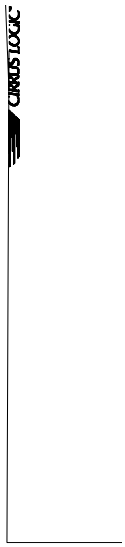
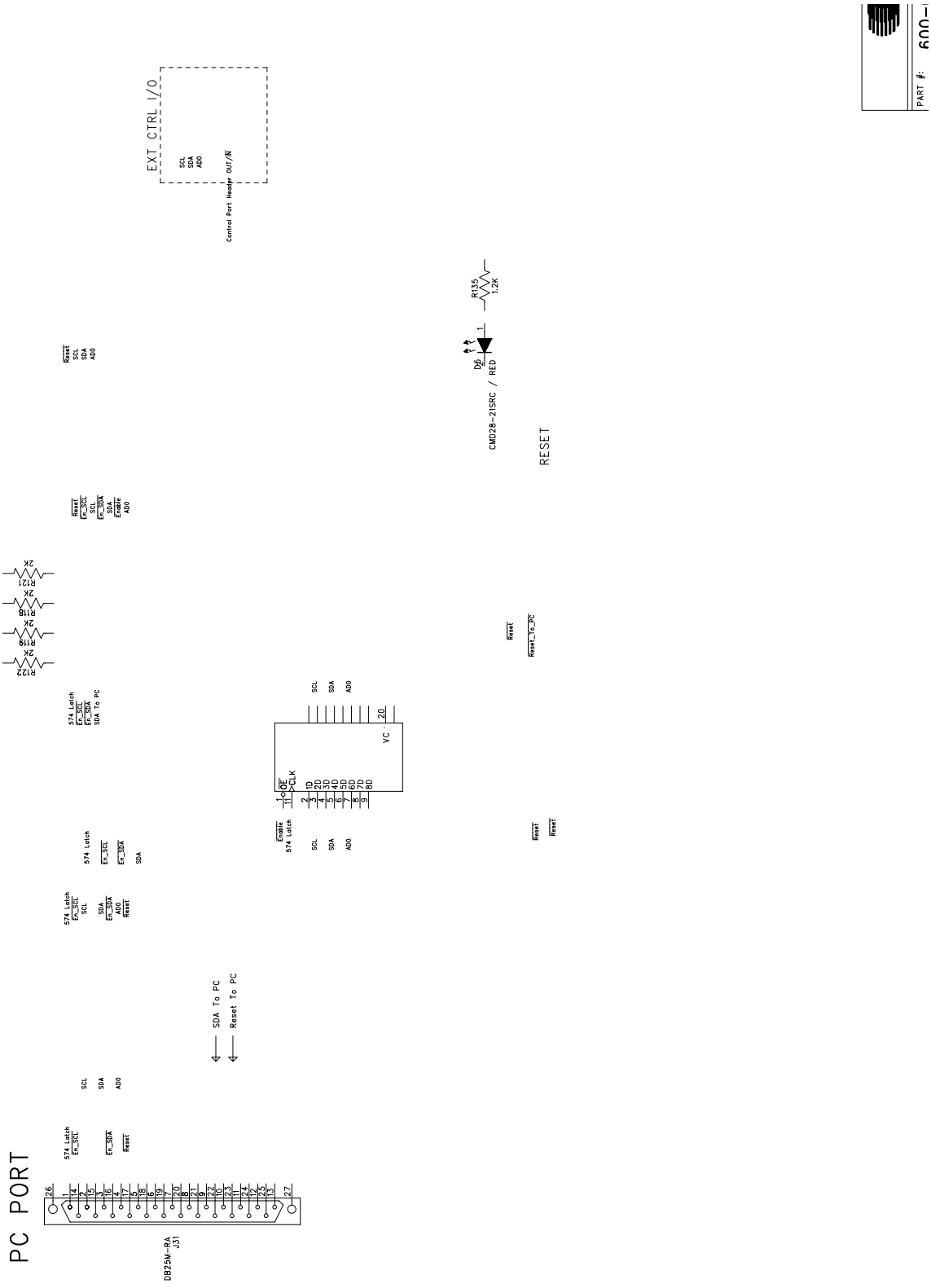


Figure 11. CS8406 S/PDIF Transmitter, Schematic Sheet 6




PART #: 6009-
EXT CTRL I/O
SCL
SDA
ADD
Control Port Header OUT/AR
R135
1.2K
D6
CMD28-21SRC / RED
RESET
Reset
SCL
SDA
ADD
Reset
En_SCL
En_SDA
SDA
Enable
ADD
R121
2K
R118
2K
R119
2K
R122
2K
574 Latch
En_SCL
En_SDA
SDA To PC
574 Latch
En_SCL
SCL
574 Latch
En_SDA
SDA
ADD
Reset
574 Latch
En_SCL
574 Latch
En_SDA
SDA
ADD
Reset
Enable
574 Latch
OE
CLK
1D
2D
3D
4D
5D
6D
7D
8D
VC
20
SCL
SDA
ADD
Reset_To_PC
Reset
Reset
SDA To PC
Reset To PC
SCL
SDA
ADD
PC PORT
574 Latch
En_SCL
En_SDA
Reset
26
1
14
2
15
3
16
4
17
5
18
6
19
7
20
8
21
9
22
10
23
11
24
12
25
13
27
DB25M-RA
J31

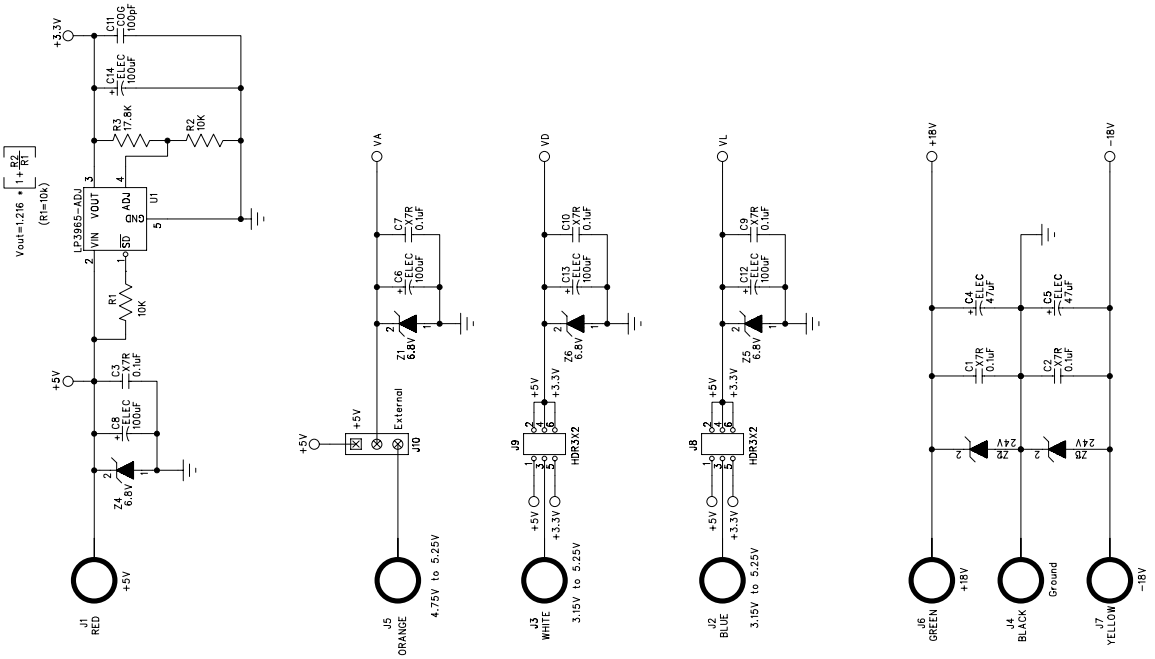
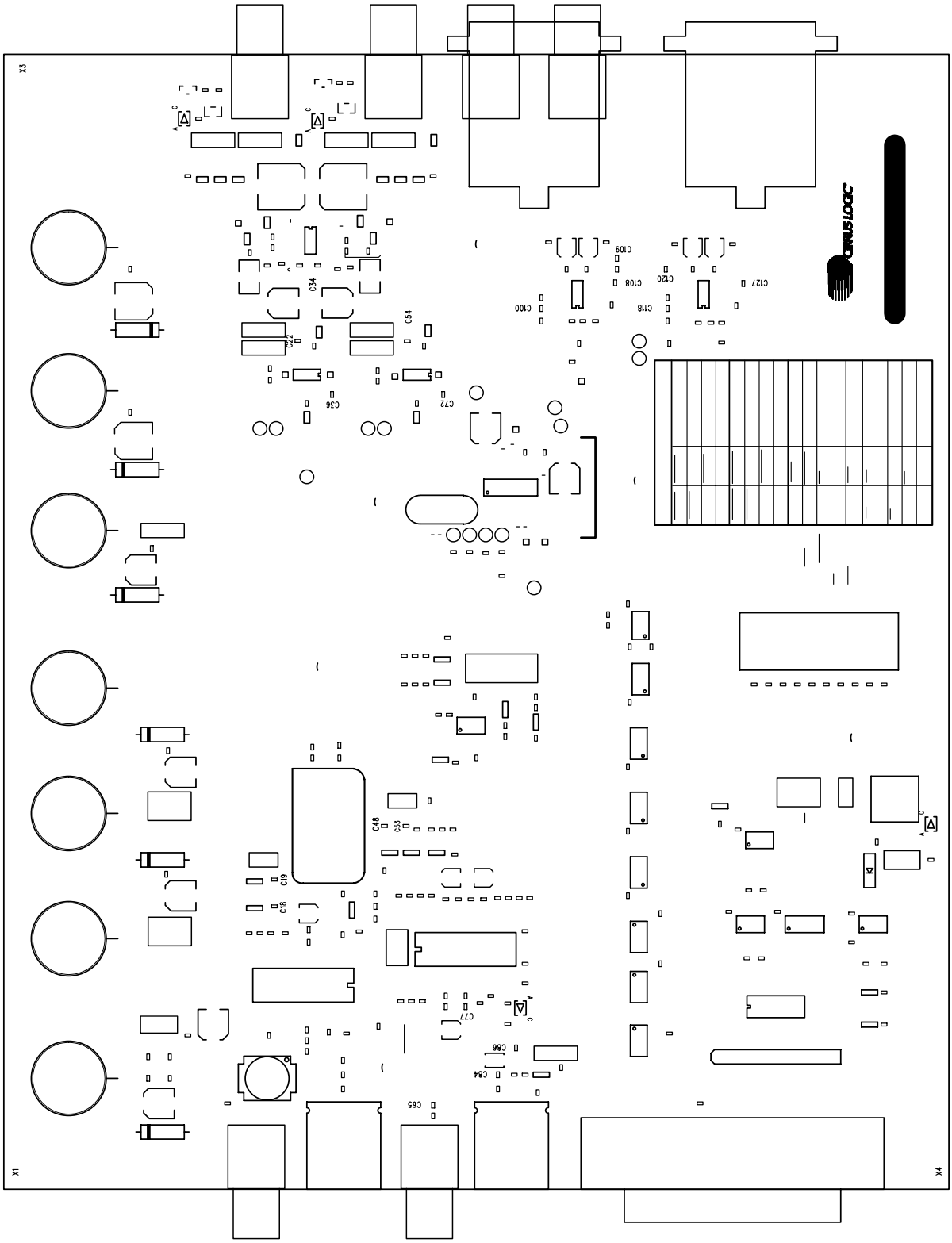
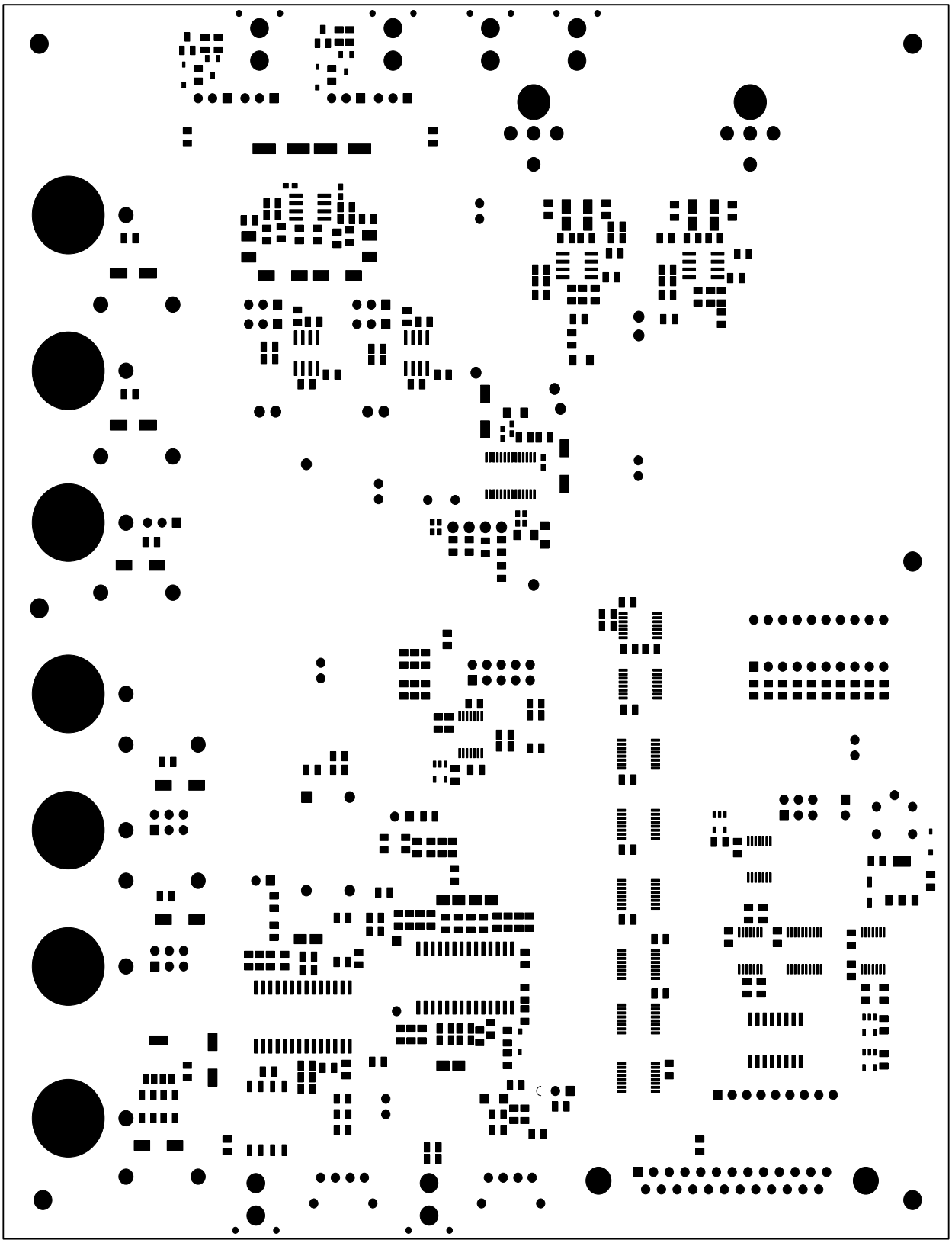
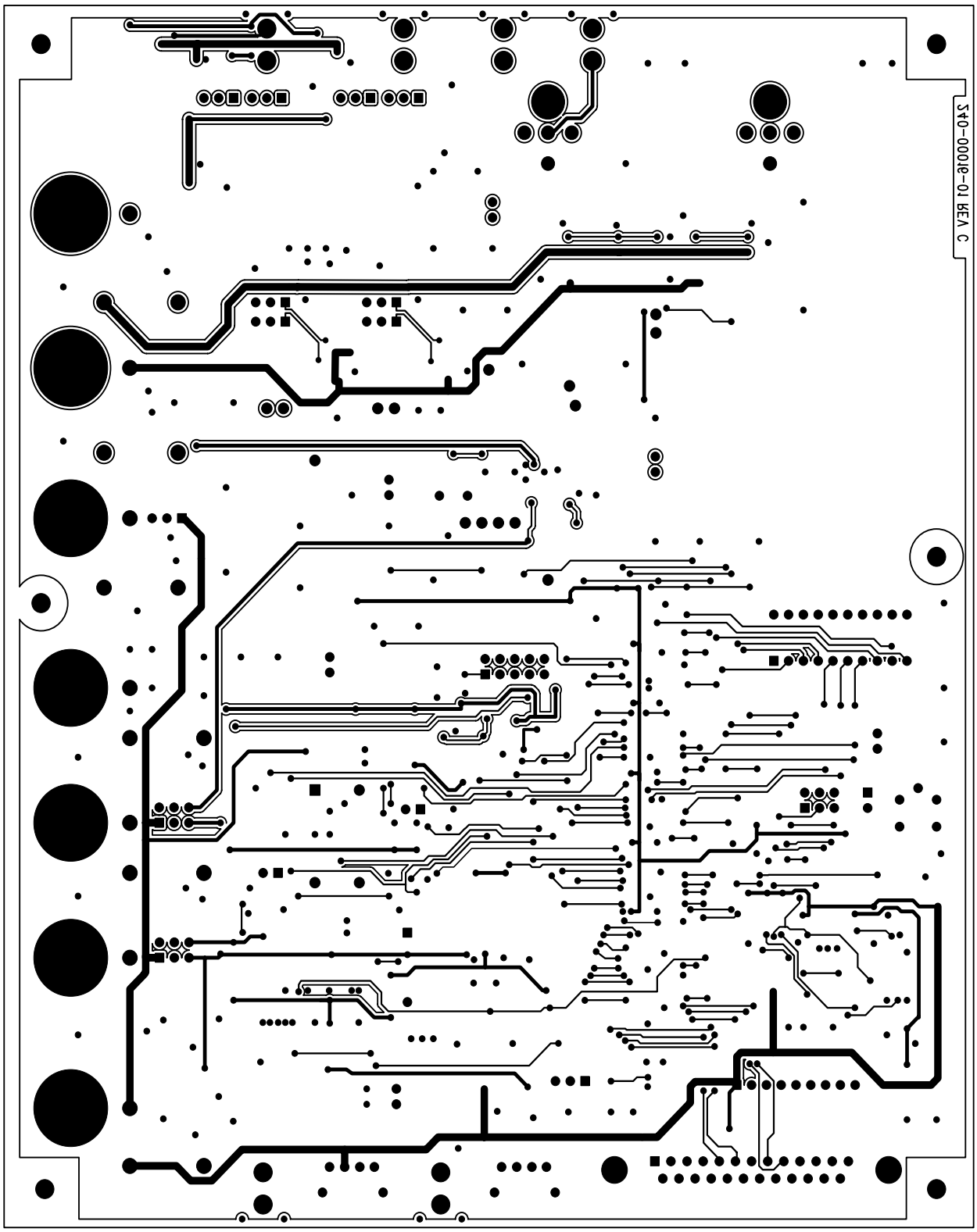


Figure 15. Power, Schematic Sheet 10


X3
X1
X4
C34
C54
C22
C36
C72
C109
C108
C120
C127
C100
C118
C48
C53
C19
C18
C77
C86
C84
C65
K1





CDB4272 (240-00016-01 REV C)

6. APPENDIX

Complete Analog Input Buffer Schematic